

Exhibit 1

Exhibit A
ACQIS's Preliminary Infringement Contentions for U.S. Patent No. 9,529,768
Sony PlayStation 4

The chart below identifies where each element of the asserted claims of U.S. Patent No. 9,529,768 (“’768 patent”) is found in the Sony PlayStation 4 series console (all models of PlayStation 4, including the PlayStation 4 Slim (including but not limited to CUH-2xxx models), PlayStation 4 Pro (including but not limited to CUH-7xxx models), and PlayStation 4 (including but not limited to CUH-1xxx models), are accused and are collectively referred to herein as “PlayStation 4” and “Accused Products”). ACQIS contends that all PlayStation 4 series consoles made, used, tested, offered for sale, sold, or imported into the United States by Sony, that share the features detailed below with reference to various exemplary PlayStation 4 models, infringed at least claims 1, 2, 13, and 17 of the ’768 patent in the manner charted herein. Specifically, all PlayStation 4 series consoles that include PCIe functionality infringed as set forth below.

This chart contains evidence relating to various PlayStation 4 models, including the PlayStation 4 Slim (CUH-2xxx), PlayStation 4 Pro (CUH-7xxx), and PlayStation 4 (CUH-1xxx), with emphasis on the PlayStation 4 Slim but including additional evidence regarding other models as well. The features of these products that are relevant to infringement are common across all PlayStation 4 models. ACQIS reserves the right to identify additional accused PlayStation 4 products based on information obtained in discovery.

ACQIS’s contentions are not limited to the PCIe implementations discussed below. ACQIS does not possess information regarding the specific manner in which all of the Accused Products utilize PCIe functionality, beyond the uses discussed below. ACQIS contends that all implementations of PCIe in the Accused Products infringed for the reasons set forth herein. ACQIS reserves the right to supplement and/or amend its contentions to provide further specificity based on information obtained in discovery.

Claim Language	Infringement Evidence
1. A computer, comprising:	<p>The PlayStation 4 is a computer running Orbis OS, a modified version of FreeBSD 9.0, as its operating system.</p> <p>https://www.extremetech.com/gaming/159476-ps4-runs-orbis-os-a-modified-version-of-freebsd-thats-similar-to-linux; https://en.wikipedia.org/wiki/PlayStation_4_system_software.</p>

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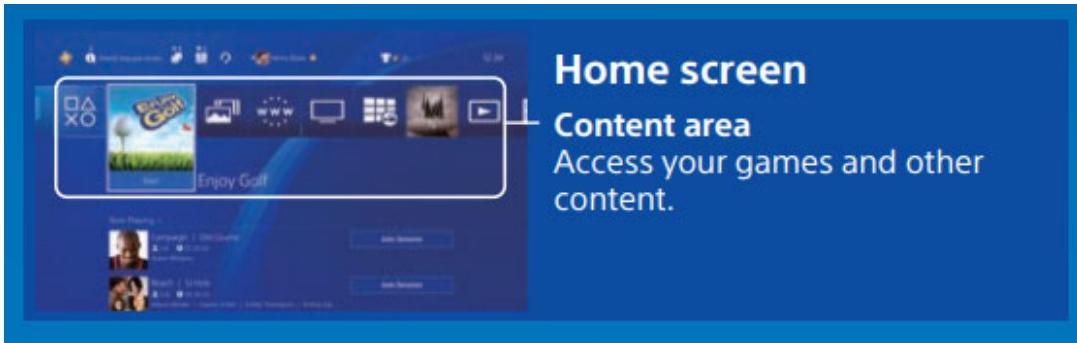
Claim Language	Infringement Evidence
	 <p data-bbox="629 791 1769 824">https://direct.playstation.com/en-us/consoles/console/playstation4-1tb-console.3003348.</p>  <p data-bbox="1298 905 1552 946">Home screen</p> <p data-bbox="1298 954 1488 987">Content area</p> <p data-bbox="1298 987 1742 1068">Access your games and other content.</p> <p data-bbox="629 1240 1531 1272">https://manuals.playstation.net/document/pdf/CUH-2215A-5.5_1.pdf.</p>

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	 <p>Home screen Content area The content that you have started is listed in most recent order from left to right.</p> <p>https://manuals.playstation.net/document/pdf/CUH-1001A-1.5_1.pdf.</p>
[1.a] an integrated central processing unit, interface controller and Phase-Locked Loop (PLL) clock circuitry in a single chip;	<p>The PlayStation 4 contains an integrated central processing unit, interface controller and Phase-Locked Loop (PLL) clock circuitry in a single chip.</p> <p>The PlayStation 4 includes a Sony Interactive Entertainment Inc. (SIEI) single-chip custom processor, e.g., the CXD90059GB in the PlayStation 4 Slim, consisting of a CPU and GPU integrated on a single chip. All eight CPU cores and the GPU are on the same die.</p>

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Claim Language	Infringement Evidence
	 <p data-bbox="625 1054 1353 1095">Teardown photograph of processor chip from PS4 Slim.</p>

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	<table border="1"><tr><td data-bbox="635 344 1178 409">Product name</td><td data-bbox="1178 344 1670 409">PlayStation®4</td></tr><tr><td data-bbox="635 442 1178 507">Product code</td><td data-bbox="1178 442 1670 507">CUH-2000 series</td></tr><tr><td data-bbox="635 540 1178 703">Main processor</td><td data-bbox="1178 540 1670 703"><p>Single-chip custom processor CPU : x86-64 AMD "Jaguar", 8 cores GPU : 1.84 TFLOPS, AMD Radeon™ based graphics engine</p></td></tr><tr><td data-bbox="635 736 1178 801">Memory</td><td data-bbox="1178 736 1670 801">GDDR5 8GB</td></tr><tr><td data-bbox="635 833 1178 899">Storage size*</td><td data-bbox="1178 833 1670 899">500GB, 1TB</td></tr></table> <p data-bbox="625 931 1860 997">https://www.playstation.com/en-us/ps4/tech-specs/ (regarding PlayStation 4 Slim) (annotations added).</p> <p data-bbox="625 1029 1924 1095">The PlayStation 4 Pro includes a CXD90044GB processor. <i>See</i> https://www.techpowerup.com/gpu-specs/playstation-4-pro-gpu.c2876.</p>	Product name	PlayStation®4	Product code	CUH-2000 series	Main processor	<p>Single-chip custom processor CPU : x86-64 AMD "Jaguar", 8 cores GPU : 1.84 TFLOPS, AMD Radeon™ based graphics engine</p>	Memory	GDDR5 8GB	Storage size*	500GB, 1TB
Product name	PlayStation®4										
Product code	CUH-2000 series										
Main processor	<p>Single-chip custom processor CPU : x86-64 AMD "Jaguar", 8 cores GPU : 1.84 TFLOPS, AMD Radeon™ based graphics engine</p>										
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Storage size*	500GB, 1TB										

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	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td data-bbox="650 360 967 393">Product name</td><td data-bbox="967 360 1664 393">PlayStation®4 Pro</td></tr> <tr> <td data-bbox="650 442 967 474">Product code</td><td data-bbox="967 442 1664 474">CUH-7000 series</td></tr> <tr> <td data-bbox="650 523 967 556">Main processor</td><td data-bbox="967 523 1664 556">Single-chip custom processor</td></tr> <tr> <td data-bbox="650 572 967 605"></td><td data-bbox="967 572 1664 605">CPU: x86-64 AMD "Jaguar", 8 cores</td></tr> <tr> <td data-bbox="650 638 967 670"></td><td data-bbox="967 638 1664 670">GPU: 4.20 TFLOPS, AMD Radeon™ based graphics engine</td></tr> <tr> <td data-bbox="650 719 967 752">Memory</td><td data-bbox="967 719 1664 752">GDDR5 8GB</td></tr> <tr> <td data-bbox="650 801 967 833">Storage size*</td><td data-bbox="967 801 1664 833">1TB</td></tr> </table> <p data-bbox="629 915 1949 948">https://www.playstation.com/en-us/ps4/tech-specs/ (regarding PlayStation 4 Pro) (annotations added).</p> <p data-bbox="629 980 1495 1046">The original PlayStation 4 includes a CXD90026BG processor. <i>See</i> https://www.techpowerup.com/gpu-specs/playstation-4-gpu.c2085.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td data-bbox="650 1095 967 1127">Specifications</td> <td data-bbox="967 1095 1664 1127"></td> </tr> <tr> <td data-bbox="650 1127 967 1160">Product Code</td><td data-bbox="967 1127 1664 1160">CUH-1000A</td></tr> <tr> <td data-bbox="650 1160 967 1192">Stock Code</td><td data-bbox="967 1160 1664 1192">CUH-1000A Series</td></tr> <tr> <td data-bbox="650 1192 967 1225">Main Processor</td><td data-bbox="967 1192 1664 1225">Single-Chip Processor CPU: x86-64 AMD "Jaguar" 8 Cores</td></tr> <tr> <td data-bbox="650 1225 967 1258">GPU</td><td data-bbox="967 1225 1664 1258">1.84 TFLOPS, AMD next-generation Radeon based graphics engine</td></tr> <tr> <td data-bbox="650 1258 967 1290">Memory</td><td data-bbox="967 1258 1664 1290">GDDR 8GB</td></tr> </table> <p data-bbox="629 1339 1949 1372">https://www.comx-computers.co.za/CUH-1000A-specifications-110924.htm (regarding PlayStation 4)</p>	Product name	PlayStation®4 Pro	Product code	CUH-7000 series	Main processor	Single-chip custom processor		CPU: x86-64 AMD "Jaguar", 8 cores		GPU: 4.20 TFLOPS, AMD Radeon™ based graphics engine	Memory	GDDR5 8GB	Storage size*	1TB	Specifications		Product Code	CUH-1000A	Stock Code	CUH-1000A Series	Main Processor	Single-Chip Processor CPU: x86-64 AMD "Jaguar" 8 Cores	GPU	1.84 TFLOPS, AMD next-generation Radeon based graphics engine	Memory	GDDR 8GB
Product name	PlayStation®4 Pro																										
Product code	CUH-7000 series																										
Main processor	Single-chip custom processor																										
	CPU: x86-64 AMD "Jaguar", 8 cores																										
	GPU: 4.20 TFLOPS, AMD Radeon™ based graphics engine																										
Memory	GDDR5 8GB																										
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Specifications																											
Product Code	CUH-1000A																										
Stock Code	CUH-1000A Series																										
Main Processor	Single-Chip Processor CPU: x86-64 AMD "Jaguar" 8 Cores																										
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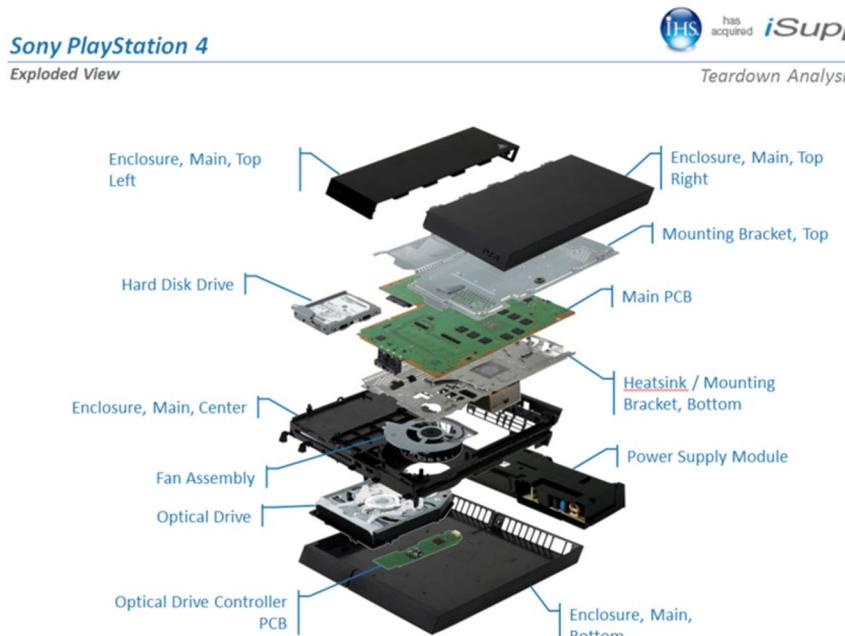
Claim Language	Infringement Evidence
	<p>(annotations added).</p>  <p>Sony PlayStation 4 Exploded View</p> <p>Copyright © 2013 iSuppli Corporation – a Company Which was Acquired by IHS, Inc.</p> <p>https://www.psdevwiki.com/ps4/File:PS4_-_Exploded_View.png.</p> <p>The Sony CXD processor in each PlayStation 4 model contains an integrated central processing unit, interface controller and PLL clock circuitry in a single chip. As shown below, the Sony processor's "Liverpool" APU includes a x4 PCIe interface on-chip.</p>

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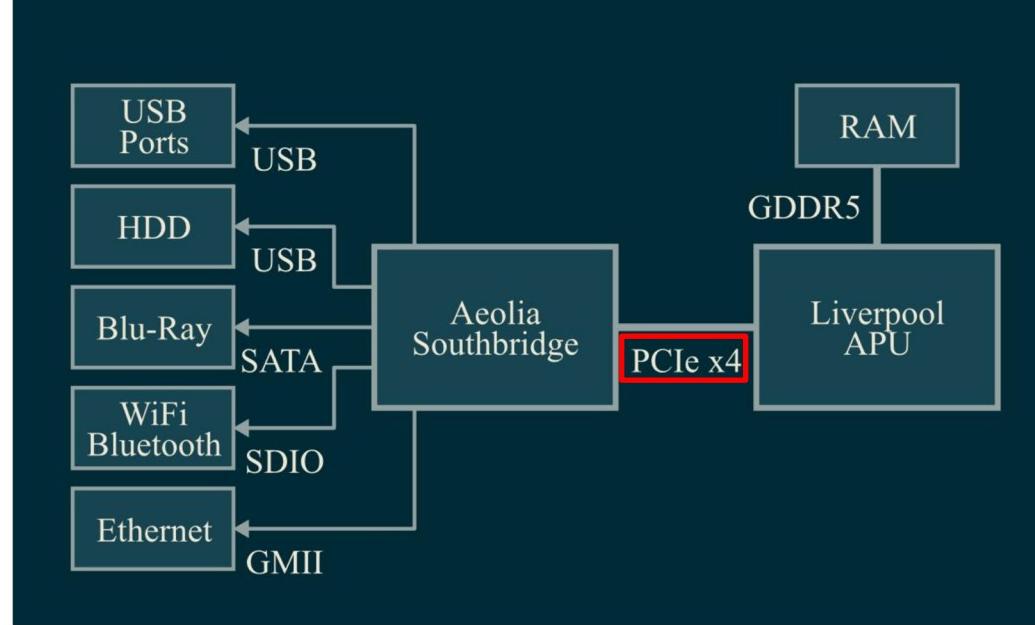
Claim Language	Infringement Evidence
	 <p>The diagram illustrates the internal architecture of the Sony PlayStation 4. At the center is the Aeolia Southbridge chip. It connects to several peripheral components via different buses:</p> <ul style="list-style-type: none">USB Ports: Connected via USB.HDD: Connected via USB.Blu-Ray: Connected via SATA.WiFi Bluetooth: Connected via SDIO.Ethernet: Connected via GMII. <p>On the right side of the diagram, the Liverpool APU is shown connected to the Aeolia Southbridge via a PCIe x4 connection. The Liverpool APU is also connected to RAM via GDDR5.</p> <p>http://www.nextgenupdate.com/forums/ps4-mods-cheats/936464-full-review-ps4-hacking-presentation-ccc-talk-team-fail0verflow.html (annotations added); https://www.youtube.com/watch?v=-AoHGJ1g9aM.</p>

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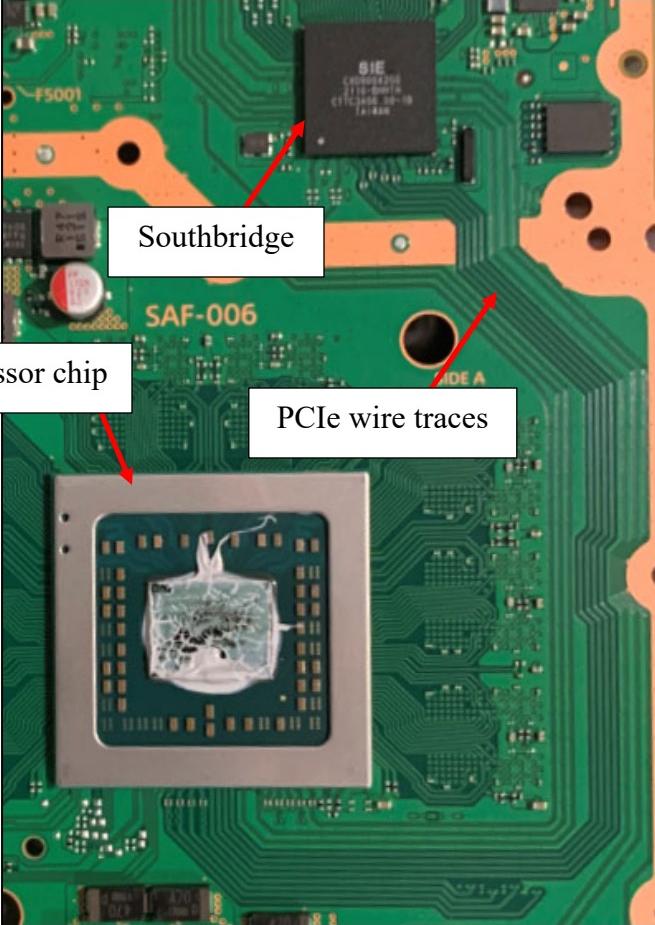
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	 <p data-bbox="629 1302 1902 1339">Teardown photograph of processor-to-southbridge connection from PS4 Slim (annotations added).</p>

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	<p>Because each Sony processor, e.g., the CXD90059GB, supports on-chip PCIe, it necessarily contains one or more logic blocks to implement the PCIe functionality, i.e., a PCIe controller and related circuitry found in the Physical Layer (PHY). This logic block (or plurality of logic blocks) is, and/or is part of, an “interface controller” within the meaning of this limitation. ACQIS does not possess specific information regarding the specific PCIe controller(s) and PHY(s) used in the PlayStation 4 models or their respective Sony processors. ACQIS reserves the right to supplement and/or amend its contentions to provide further specificity based on information obtained in discovery.</p> <p>As discussed below with respect to limitation [1.c], each Sony processor, e.g., the CXD90059GB, includes PLL clock circuitry, including at least in the PHY(s) associated with the PCIe controller(s).</p>
[1.b] a Low Voltage Differential Signal (LVDS) channel directly extending from the interface controller to convey address and data bits of a Peripheral Component Interconnect (PCI) bus transaction in a serial form, wherein the first LVDS channel comprises a first unidirectional, differential signal pair to convey data in a first direction and a second unidirectional, differential signal pair to convey data in a second, opposite direction; and	<p>The Sony CXD processor found in the PlayStation 4, e.g., the CXD90059GB in the PlayStation 4 Slim, which includes an integrated CPU, interface controller and PLL clock circuitry, has a Low Voltage Differential Signal (LVDS) channel directly extending from the interface controller.</p> <p>As discussed above with respect to limitation [1.a], each Sony CXD processor includes a x4 on-chip PCIe interface, as shown below.</p>

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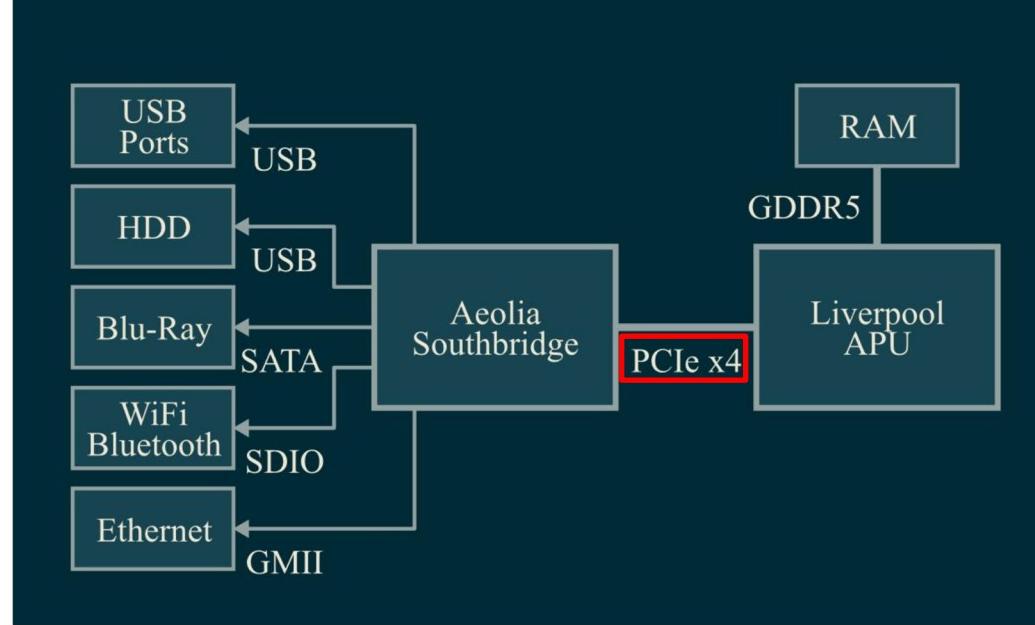
Claim Language	Infringement Evidence
	 <p>The diagram illustrates the internal architecture of the Sony PlayStation 4. At the center is the Aeolia Southbridge chip. It connects to several peripheral components via different buses:</p> <ul style="list-style-type: none">USB Ports: Connected via USB.HDD: Connected via USB.Blu-Ray: Connected via SATA.WiFi Bluetooth: Connected via SDIO.Ethernet: Connected via GMII. <p>To the right of the Southbridge is the Liverpool APU, which contains RAM (GDDR5) and is connected via a PCIe x4 interface. A red box highlights the PCIe x4 connection.</p> <p>http://www.nextgenupdate.com/forums/ps4-mods-cheats/936464-full-review-ps4-hacking-presentation-ccc-talk-team-fail0verflow.html (annotations added); https://www.youtube.com/watch?v=-AoHGJ1g9aM.</p>

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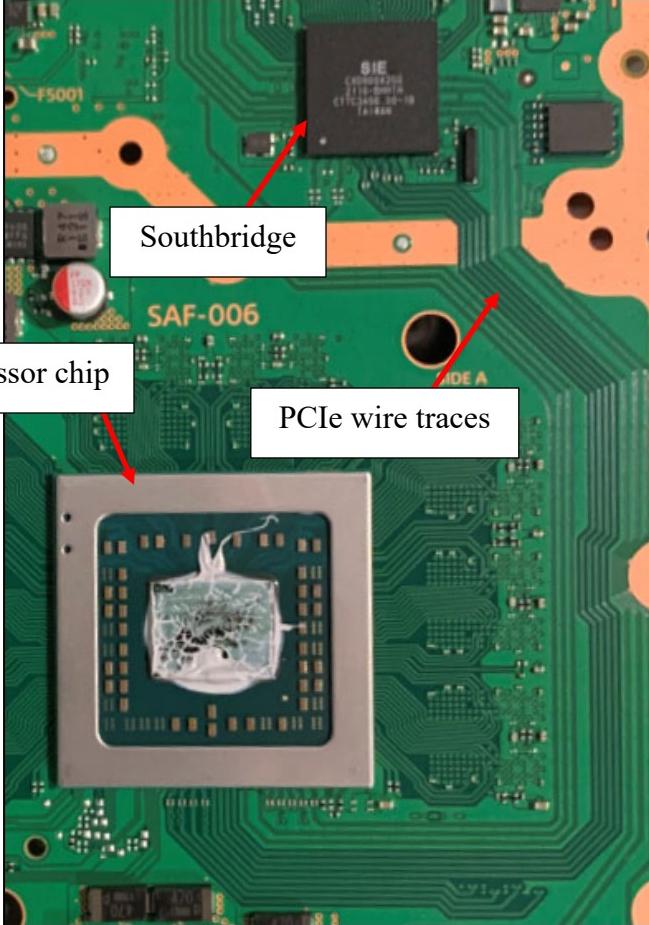
Claim Language	Infringement Evidence
	 <p data-bbox="958 339 1607 1264">A photograph of a green printed circuit board (PCB) from a Sony PlayStation 4 Slim. The board features several components: a large central processor chip, a smaller southbridge chip labeled 'SIE CXD3082P6 2110-B007A CTC3408-B01-10' (part number), and a red cylindrical component labeled 'SAF-006'. Red arrows point to three specific areas with white callout boxes: 'Southbridge' points to the southbridge chip, 'Processor chip' points to the central processor, and 'PCIe wire traces' points to the green printed circuit board tracks connecting the two chips.</p> <p data-bbox="629 1302 1896 1334">Teardown photograph of processor-to-southbridge connection from PS4 Slim (annotations added).</p> <p data-bbox="629 1375 1854 1408">The PlayStation 4 uses the Sony CXD processor's on-chip PCIe I/O for directly connecting the</p>

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	<p>southbridge to the processor chip in a four-lane PCIe configuration, as shown above. The southbridge in the PlayStation 4 Slim is the Sony CXD90042GG, as shown below.</p>  <p>Teardown photograph of southbridge from PS4 Slim.</p> <p>The southbridge chip in each PlayStation 4 model is supplied by Marvell Technology, Inc. <i>See, e.g.</i>, https://www.psdevwiki.com/ps4/Southbridge. PlayStation 4 models include various southbridge models, including CXD90025G (“Aeolia”), CXD90036G (“Belize”), CXD90042GG (“Baikal”), and CXD90046GG (“Belize 2”). <i>Id.</i> The functionality of each unique southbridge is identical in relevant part.</p> <p>The PCIe interface used in the PlayStation 4 for connecting the southbridge to the CPU, as described</p>

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	<p>above, has an LVDS channel directly extending from the interface controller that conveys address and data bits of a PCI bus transaction in a serial form.</p> <p>As discussed above with respect to limitation [1.a], each Sony CXD processor contains one or more logic blocks to implement the PCIe functionality, i.e., a PCIe controller and related circuitry found in the Physical Layer (PHY). The PCIe controller has an associated PHY connected to it via the PIPE interface. ACQIS does not possess specific information regarding the specific PCIe controller(s) and PHY(s) used in the PlayStation 4 or in each Sony CXD processor. ACQIS reserves the right to supplement and/or amend its contentions to provide further specificity based on information obtained in discovery.</p> <p>LVDS is central to PCIe, providing the physical transmission medium, and all implementations of PCIe utilize LVDS:</p> <p style="padding-left: 40px;">PCI Express . . . is a serial bus which uses two low-voltage differential LVDS pairs, at 2.5Gb/s in each direction [one transmit, and one receive pair]. A PCI Express link is comprised of these two unidirectional differential pairs each operating at 2.5Gbps to achieve a basic [overall] throughput of 5Gbps [before accounting for over-head].</p> <p style="padding-left: 40px;">http://www.interfacebus.com/PCI-Express-Bus-PCIe-Description.html.</p> <p>This LVDS channel comprises a first unidirectional, differential signal pair to convey data in a first direction and a second unidirectional, differential signal pair to convey data in a second, opposite direction. As shown in the exemplary PCIe illustrations below, each lane in a PCIe implementation contains a first unidirectional, differential signal pair to convey data in a first direction (i.e., the Tx pairs in the upper illustration and the signal pairs in red in the lower illustration) and a second unidirectional, differential signal pair to convey data in a second direction (i.e., the Rx signal pairs in the upper illustration and the signal pairs in yellow in the lower illustration). In a multi-lane PCIe configuration, the stream of bytes that make up a TLP go through byte striping, which distributes the</p>

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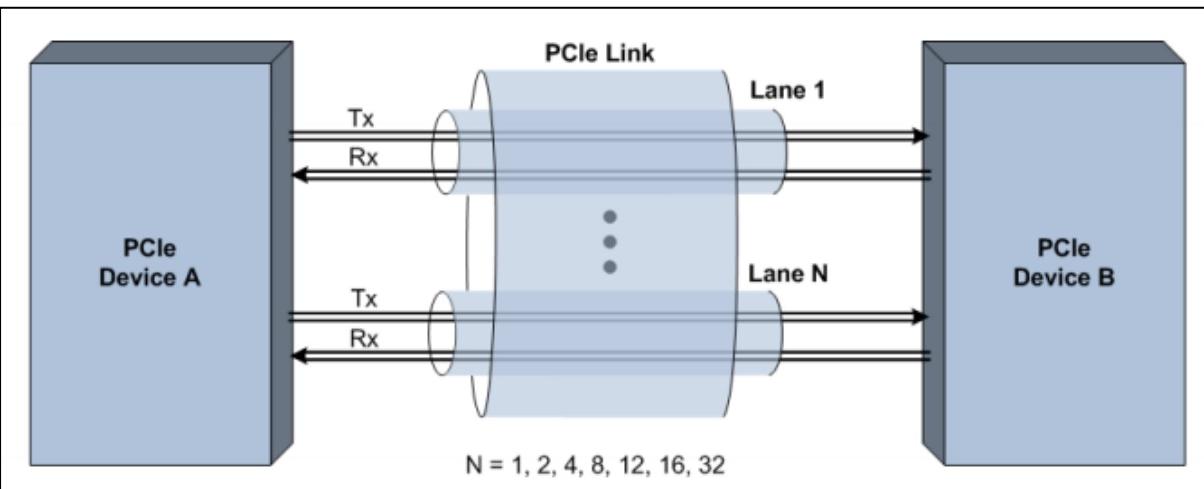
Claim Language	Infringement Evidence
	<p>bytes across the available lanes for serialization. See PCI Express Base Specification, Revision 3.0 (Nov. 10, 2010) at 195-198. The transaction's byte-oriented data (character) is encoded, serialized, and output one byte at a time per lane in the PCIe link. <i>Id.</i> Thus in PCIe, the TLP is in serial form for all link widths. <i>Id.</i></p>  <p style="text-align: center;">$N = 1, 2, 4, 8, 12, 16, 32$</p> <p><i>Silicon Labs AN562, PCI Express 3.1 Jitter Requirements (Rev. 0.2 11/15) (available at https://www.silabs.com/documents/public/application-notes/AN562.pdf), at 2.</i></p>

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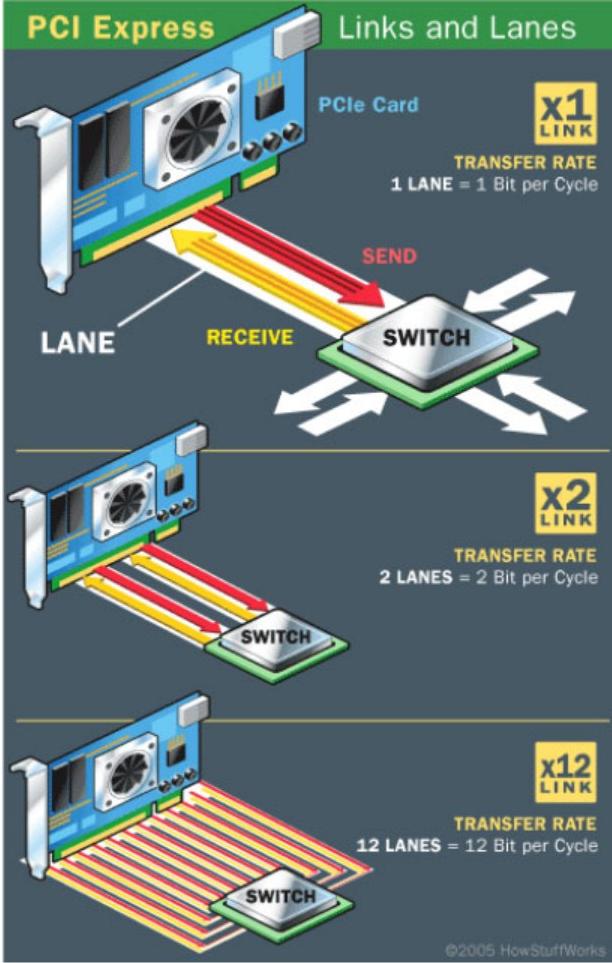
Claim Language	Infringement Evidence
	 <p>The diagram illustrates the concept of PCI Express Links and Lanes. It shows three horizontal sections representing different link widths:</p> <ul style="list-style-type: none">x1 Link: Shows a single PCIe card connected to a switch via a single lane. The transfer rate is 1 Bit per Cycle, and 1 Lane = 1 Bit per Cycle.x2 Link: Shows a single PCIe card connected to a switch via two lanes. The transfer rate is 2 Bits per Cycle, and 2 LANES = 2 Bit per Cycle.x12 Link: Shows a single PCIe card connected to a switch via twelve lanes. The transfer rate is 12 Bits per Cycle, and 12 LANES = 12 Bit per Cycle. <p>Each section includes a PCIe card with a fan, a red and yellow ribbon cable representing the lane(s), and a green switch component. The text "PCI Express" is at the top left, and "Links and Lanes" is at the top right. The copyright notice "©2005 HowStuffWorks" is at the bottom right of the diagram area.</p> <p>https://computer.howstuffworks.com/pci-express.htm.</p>

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	<p>The data that is transmitted in a serial PCIe bus transaction includes address and data bits of a PCI bus transaction. The transaction layer packets (TLPs) used for PCIe data transmission include both address and data bits of a PCI bus transaction.</p> <div data-bbox="629 486 1742 1036" style="border: 1px solid black; padding: 10px;"><p>The Address Element</p><p>The address elements of the TLP provide the address to select specific bytes within the memory and I/O address spaces. The address elements also provide the ID Routing and the register address to select the specific bytes of the configuration register block in the configuration address space. Finally, address elements also provide the ID and Implied Routing for the message address space.</p><p><i>Header field of TLP contains:</i></p><p>ADDRESS: The “typical” address bits for memory and I/O address space. The address can also be used in message vendor-defined transaction packets.</p></div> <p><i>The Complete PCI Express Reference, Intel Press (2003), at 218.</i></p> <div data-bbox="629 1139 1742 1321" style="border: 1px solid black; padding: 10px;"><p>The Data Element</p><p>The data element of the transaction packet provides the actual data being accessed.</p></div> <p><i>The Complete PCI Express Reference, Intel Press (2003), at 220.</i></p>

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	<p style="text-align: center;">Figure 6.4 64-bit Address Memory Request Header</p>
	<p style="text-align: center;">Figure 6.5 32-bit Address Memory Request Header</p>

Introduction to PCI Express – A Hardware and Software Developers Guide, Intel Press (2003), at 100.

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	<p>Further, PCIe is backwards compatible with PCI, as PCI is described in the PCI Local Bus Specification. In PCIe, “[k]ey PCI attributes, such as its usage model, load-store architecture, and software interfaces, are maintained, whereas its parallel bus implementation is replaced by a highly scalable, fully serial interface.” PCI Express Base Specification, Revision 3.0 (Nov. 10, 2010) (“PCIe 3.0 Spec.”) at 37. PCIe maintains a “PCI compatible software model,” providing:</p> <div style="border: 1px solid black; padding: 10px; margin-left: 20px;"><p><input checked="" type="checkbox"/> PCI compatible software model:</p><ul style="list-style-type: none">• Ability to enumerate and configure PCI Express hardware using PCI system configuration software implementations with no modifications• Ability to boot existing operating systems with no modifications• Ability to support existing I/O device drivers with no modifications• Ability to configure/enable new PCI Express functionality by adopting the PCI configuration paradigm</div> <p>PCIe 3.0 Spec. at 38.</p> <p>A Peripheral Component Interconnect (PCI) bus transaction, in accordance with the industry standard PCI Local Bus Specification, Revision 2.2 (Dec. 18, 1998) (“PCI Specification”), for communication with an interconnected peripheral component (a “PCI transaction”) consists of an address phase and one or more data phases. (<i>See, e.g., PCI Specification</i> at 9, 301.) Example transactions include input/output (I/O) read, I/O write, memory read, memory write, configuration read, and configuration write. (<i>See, e.g., PCI Specification</i> at 21-23.) A PCI transaction facilitates communication and data transfer among computer components, such as processors, memory, and peripheral devices. (<i>See, e.g., PCI Specification</i> at 1, 3.) PCI transactions include a set of address bits, a set of data bits, a set of command bits, and a set of byte enable information bits. (<i>See, e.g., PCI Specification</i> at 9-10.) The</p>

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Claim Language	Infringement Evidence
	<p>address bits allow one component to communicate with another specific component. (<i>See, e.g., PCI Specification</i> at 9, 27-29.) The data bits transfer data from one component to another. (<i>See, e.g., PCI Specification</i> at 9.) The command bits indicate the type of transaction (such as memory, I/O, or configuration) and control the transaction. (<i>See, e.g., PCI Specification</i> at 21-24.) The byte enable information bits indicate the size of the data transfer and the bytes in the data transfer that contain valid data. (<i>See, e.g., PCI Specification</i> at 10, 28.)</p> <p>The PCIe Base Specification Revision 1.0a (Apr. 15, 2003) (“PCIe Specification”), utilizes transactions to facilitate communication and data transfer among computer components. (<i>See, e.g., PCIe Specification</i> at 27.) PCIe transactions are defined in the PCIe Transaction Layer. (<i>See, e.g., PCIe Specification</i> at 36.) PCIe transactions include read and write transactions. (<i>See, e.g., PCIe Specification</i> at 42.) PCIe transactions are communicated using bits. (<i>See, e.g., PCIe Specification</i> at 44.) PCIe employs the three transaction types (memory, I/O, and configuration) described in the PCI Local Bus Specification. (<i>See, e.g., PCIe Specification</i> at 36, 45.) PCIe provides a PCI-compatible software model. (<i>See, e.g., PCIe Specification</i> at 27.)</p> <p>PCIe transactions include command bits to indicate the type of transaction (such as memory, I/O, or configuration) and control the transaction. (<i>See, e.g., PCIe Specification</i> at 44-47.) PCIe transactions include address bits to allow one component to communicate with another specific component. (<i>See, e.g., PCIe Specification</i> at 49-50; <i>see also, e.g., The Complete PCI Express Reference</i>, Intel Press (2003), at 218.) PCIe transactions include data bits to transfer data between components. (<i>See, e.g., PCIe Specification</i> at 44; <i>see also, e.g., The Complete PCI Express Reference</i>, Intel Press (2003), at 220.) PCIe transactions include byte enable information to indicate the size of the data transfer and the bytes in the data transfer that contain valid data. (<i>See, e.g., PCIe Specification</i> at 52-53; <i>see also, e.g., Introduction to PCI Express – A Hardware and Software Developers Guide</i>, Intel Press (2003), at 100.)</p> <p>A PCIe transaction therefore provides a Peripheral Component Interconnect (PCI) bus transaction in accordance with the industry standard PCI Local Bus Specification, for communication with an</p>

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	<p>interconnected peripheral component. A PCIe transaction provides address bits, data bits, and byte enable information bits of a Peripheral Component Interconnect (PCI) bus transaction.</p> <p>To the extent that Sony contends that a PCIe transaction does not provide a Peripheral Component Interconnect (PCI) bus transaction or address bits, data bits, and/or byte enable information bits of a Peripheral Component Interconnect (PCI) bus transaction, a PCIe transaction satisfies these claim elements under the doctrine of equivalents. A PCIe transaction—including its address, data, and byte enable information bits—performs substantially the same function, in substantially the same way, to obtain the same result as a PCI transaction, including its address, data, and byte enable information bits. A PCIe transaction—including its address, data, and byte enable information bits—is not substantially different from a PCI transaction, including its address, data, and byte enable information bits.</p> <p>A PCI transaction and a PCIe transaction both perform the function of facilitating communication among components in a computer system. A PCI transaction and a PCIe transaction perform this function by utilizing address bits, data bits, and byte enable bits. In both PCI and PCIe transactions, address bits allow one component to communicate with another specific component. In both PCI and PCIe transactions, data bits transfer data from one component to another. In both PCI and PCIe transactions, command bits indicate the type of transaction and control the transaction. In both PCI and PCIe transactions, byte enable bits indicate the size of the data transfer and the bytes in the data transfer that contain valid data. A PCI transaction and a PCIe transaction therefore both perform the function of facilitating communication among components in a computer system in substantially the same way. The address bits, data bits, command bits, and byte enable information bits in a PCIe transaction do not differ substantially from the address bits, data bits, command bits, and byte enable information bits in a PCI transaction. A PCIe transaction uses substantially similar bits as a PCI transaction in order to maintain consistency and software compatibility with PCI. A PCI transaction and a PCIe transaction produce the same result of communication among components in a computer system.</p>

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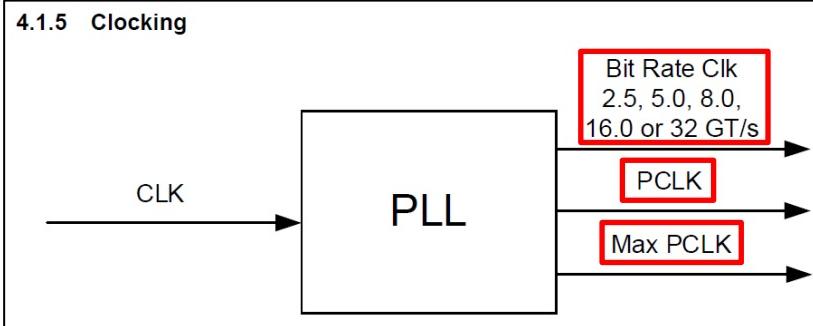
Claim Language	Infringement Evidence
<p>[1.c] wherein the PLL clock circuitry generates different clock frequencies, and the interface controller conveys the PCI bus transaction through the LVDS channel based on the different clock frequencies.</p>	<p>As discussed above with respect to limitation [1.a], the processor in the PlayStation 4, i.e., each Sony CXD processor, includes an on-chip PCIe controller and an associated PHY.</p> <p>The PHY in each Sony CXD processor, e.g., the CXD90059GB processor in the PlayStation 4 Slim, includes PLL clock circuitry. The PHY contains at least one PLL and likely contains multiple PLLs.</p> <p>Within the PHY Interface for the PCI Express Architecture (PIPE), the PLL clock circuitry generates at least two clocks at different frequencies. One frequency is used as a bitrate clock (2.5 GHz – 32 GHz, depending on the PCIe transfer rates supported; PCIe 3.x supports 8 GT/s, and PCIe 2.x supports 5 GT/s), and the other is for the PIPE interface to the rest of the PCIe controller, i.e., PCLK (or pipe_clock) at 125 MHz or 250 MHz. Additionally, the PLL clock circuitry may generate a third clock frequency which is the bitrate clock divided by 10, i.e., bit rate clk / 10. Thus, the PLL clock circuitry generates different clock frequencies, which are used to convey the PCI bus transactions through the LVDS channel.</p>  <p><i>PHY Interface for the PCI Express, SATA, USB 3.1, DisplayPort, and Converged IO Architectures, Version 5.1 (2018) (available at https://www.intel.com/content/dam/www/public/us/en/documents/white-papers/phy-interface-pci-express-sata-usb30-architectures-3.1.pdf), at 32 (annotations added).</i></p>

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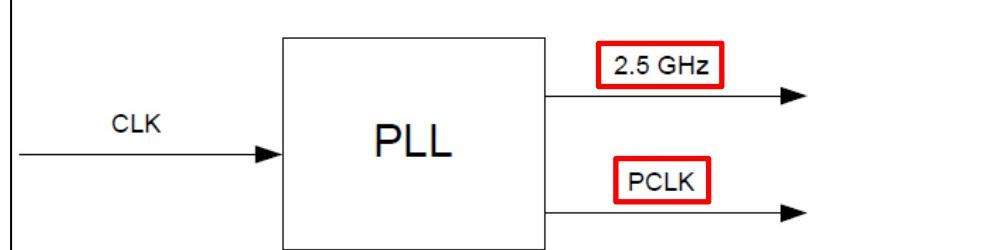
Claim Language	Infringement Evidence
	 <p data-bbox="1058 621 1769 654">Figure 6: Clocking and Power Block Diagram</p> <p data-bbox="629 727 1833 801"><i>PHY Interface for the PCI Express Architecture, Version 2.00 (2007) (available at http://www.applistar.com/wp-content/uploads/apps/pipe2_00.pdf), at 11 (annotations added).</i></p>

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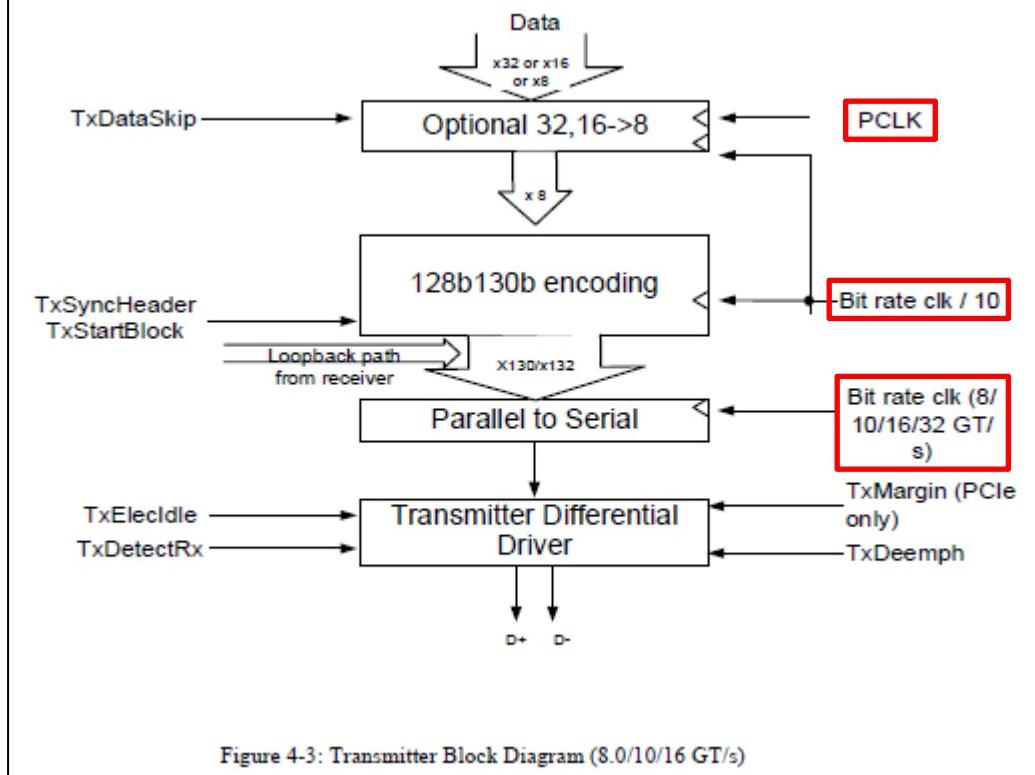
Claim Language	Infringement Evidence
	 <p>The diagram illustrates the transmitter block architecture for 8.0/10/16 GT/s. The process starts with an optional 32,16->8 bit reduction stage, followed by 128b130b encoding. A parallel-to-serial converter then converts the data into a serial stream. Finally, a transmitter differential driver produces the D+ and D- outputs. Various control signals and clock sources are also shown.</p> <p>Annotations in red boxes highlight specific components:</p> <ul style="list-style-type: none"> PCLK (Phase Lock Clock) Bit rate clk / 10 Bit rate clk (8/10/16/32 GT/s) TxMargin (PCIe only) <p>Figure 4-3: Transmitter Block Diagram (8.0/10/16 GT/s)</p> <p><i>PHY Interface for the PCI Express, SATA, USB 3.1, DisplayPort, and Converged IO Architectures, Version 5.1 (2018) (available at https://www.intel.com/content/dam/www/public/us/en/documents/white-papers/phy-interface-pci-express-sata-usb30-architectures-3.1.pdf), at 29 (annotations added).</i></p>

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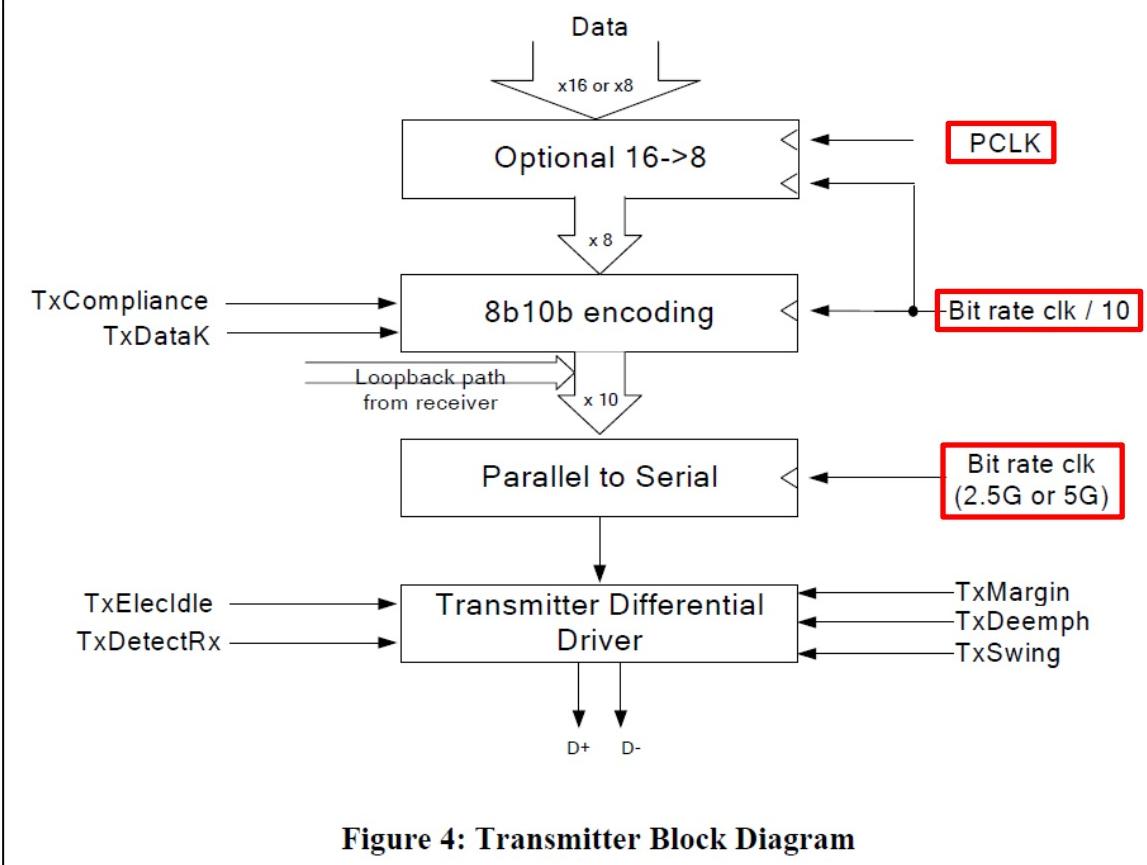
Claim Language	Infringement Evidence
	 <p>The diagram illustrates the transmitter block diagram, showing the signal flow and key components:</p> <ul style="list-style-type: none"> Data (x16 or x8) enters the Optional 16->8 block. PCLK (Provided by Sony PlayStation 4) is connected to the Optional 16->8 block. The output of the Optional 16->8 block is scaled by x 8 and then enters the 8b10b encoding block. TxClock and TxDATAK are inputs to the 8b10b encoding block. A Loopback path from receiver (x 10) is shown, indicating a feedback loop. Bit rate clk / 10 is connected to the 8b10b encoding block. The output of the 8b10b encoding block enters the Parallel to Serial block. Bit rate clk (2.5G or 5G) is connected to the Parallel to Serial block. The output of the Parallel to Serial block enters the Transmitter Differential Driver. TxEleIdle and TxDetectRx are inputs to the Transmitter Differential Driver. TxMargin, TxDemph, and TxSwing are also inputs to the Transmitter Differential Driver. The Transmitter Differential Driver outputs D+ and D-. <p>Figure 4: Transmitter Block Diagram</p> <p><i>PHY Interface for the PCI Express Architecture, Version 2.00 (2007) (available at http://www.applistar.com/wp-content/uploads/apps/pipe2_00.pdf), at 10 (annotations added).</i></p>

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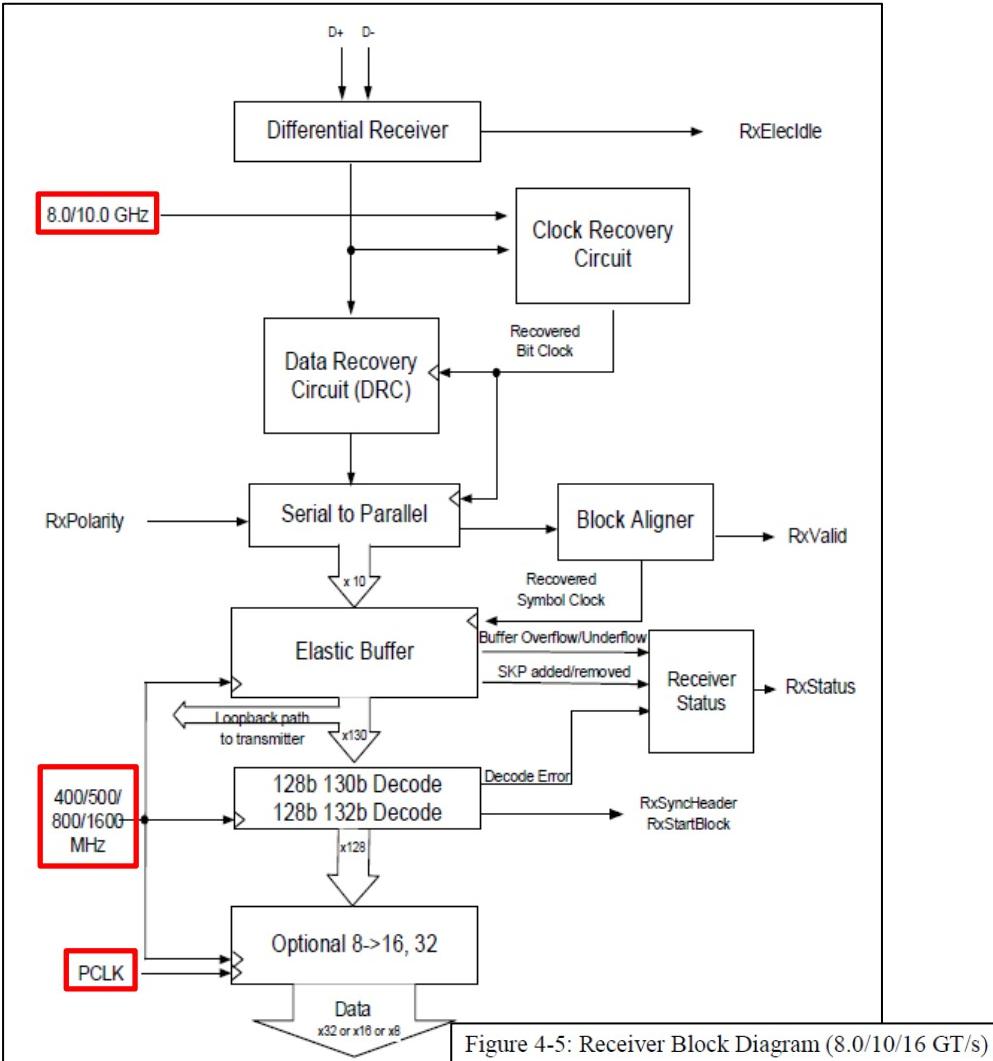
Claim Language	Infringement Evidence
	 <p>The diagram illustrates the receiver architecture for 8.0/10/16 GT/s speeds. It starts with a Differential Receiver receiving D+ and D- signals. The recovered Recovered Bit Clock is fed into the Clock Recovery Circuit. The recovered Recovered Symbol Clock is fed into the Block Aligner. The Block Aligner also receives RxPolarity and RxValid signals. The Serial to Parallel converter receives data from the Data Recovery Circuit and RxPolarity, and outputs data to the Elastic Buffer. The Elastic Buffer also receives a Loopback path to transmitter signal. The 128b 130b Decode and 128b 132b Decode blocks receive data from the Elastic Buffer and PCLK. The 128b 130b Decode block also provides a Decode Error signal. The Optional 8->16, 32 converter receives data from the 128b 132b Decode block and PCLK. The final output is Data at x32 or x16 or x8 rates. The Receiver Status block monitors the buffer overflow/underflow and provides RxSyncHeader and RxStartBlock signals.</p> <p>Figure 4-5: Receiver Block Diagram (8.0/10/16 GT/s)</p>

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	<p><i>PHY Interface for the PCI Express, SATA, USB 3.1, DisplayPort, and Converged IO Architectures</i>, Version 5.1 (2018) (available at https://www.intel.com/content/dam/www/public/us/en/documents/white-papers/phy-interface-pci-express-sata-usb30-architectures-3.1.pdf), at 31-32 (annotations added).</p>

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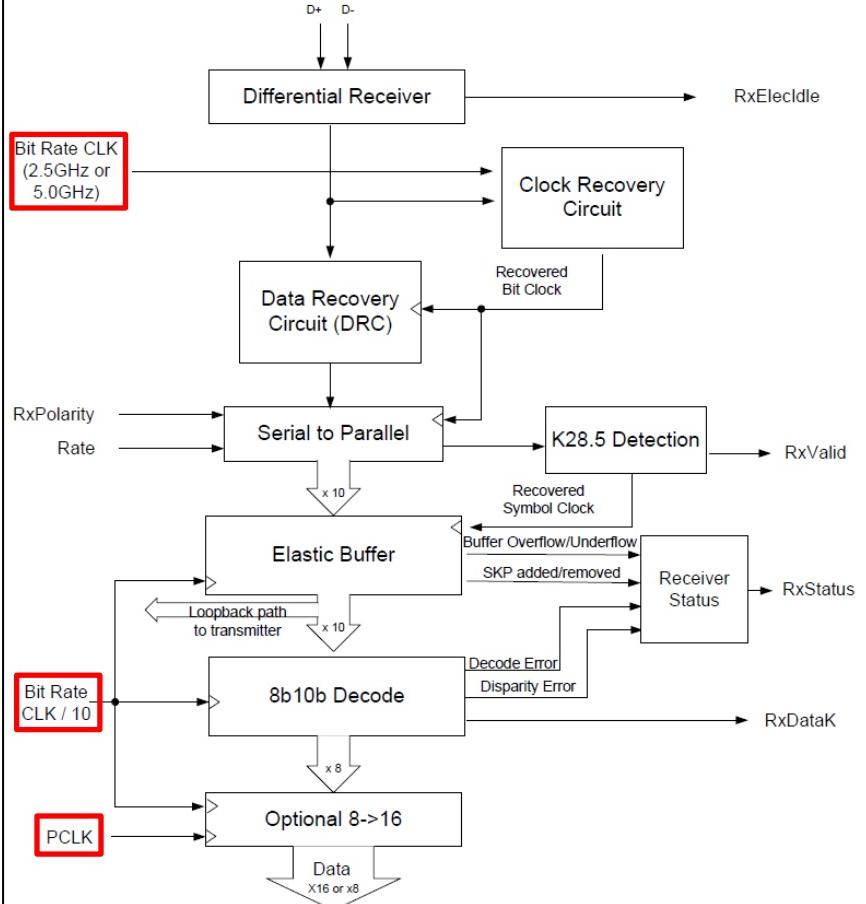
Claim Language	Infringement Evidence
	 <p style="text-align: center;">Figure 5: Receiver Block Diagram</p>

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	<p><i>PHY Interface for the PCI Express Architecture</i>, Version 2.00 (2007) (available at http://www.applistar.com/wp-content/uploads/apps/pipe2_00.pdf), at 11 (annotations added).</p> <table border="1" data-bbox="734 442 1818 1111"> <caption data-bbox="777 458 1227 491">Table 6-18. External Input Signals</caption> <thead> <tr> <th data-bbox="777 499 988 600">Name</th><th data-bbox="988 499 1094 600">Active Level</th><th data-bbox="1094 499 1622 600">Description</th><th data-bbox="1622 499 1776 600">Relevant Protocols</th></tr> </thead> <tbody> <tr> <td data-bbox="777 600 988 801">CLK</td><td data-bbox="988 600 1094 801">Edge</td><td data-bbox="1094 600 1622 801">This differential Input is used to generate the bit-rate clock for the PHY transmitter and receiver. Specs for this clock signal (frequency, jitter, ...) are implementation dependent and must be specified for each implementation. This clock may have a spread spectrum modulation.</td><td data-bbox="1622 600 1776 801">PCIe, SATA, USB, DisplayPort, Converged IO</td></tr> <tr> <td data-bbox="777 801 988 1090">PCLK</td><td data-bbox="988 801 1094 1090">Rising Edge</td><td data-bbox="1094 801 1622 1090"> <p><i>This signal is relevant for "PCLK as PHY Input" mode only.</i></p> <p>All data movement across the parallel interface is synchronized to this clock. This clock operates at a frequency set by PCLK Rate. The rising edge of the clock is the reference for all signals. Spread spectrum modulation on this clock is allowed.</p> </td><td data-bbox="1622 801 1776 1090">PCIe, SATA, USB, DisplayPort, Converged IO</td></tr> </tbody> </table> <p><i>PHY Interface for the PCI Express, SATA, USB 3.1, DisplayPort, and Converged IO Architectures</i>, Version 5.1 (2018) (available at https://www.intel.com/content/dam/www/public/us/en/documents/white-papers/phy-interface-pci-express-sata-usb30-architectures-3.1.pdf), at 77.</p>	Name	Active Level	Description	Relevant Protocols	CLK	Edge	This differential Input is used to generate the bit-rate clock for the PHY transmitter and receiver. Specs for this clock signal (frequency, jitter, ...) are implementation dependent and must be specified for each implementation. This clock may have a spread spectrum modulation.	PCIe, SATA, USB, DisplayPort, Converged IO	PCLK	Rising Edge	<p><i>This signal is relevant for "PCLK as PHY Input" mode only.</i></p> <p>All data movement across the parallel interface is synchronized to this clock. This clock operates at a frequency set by PCLK Rate. The rising edge of the clock is the reference for all signals. Spread spectrum modulation on this clock is allowed.</p>	PCIe, SATA, USB, DisplayPort, Converged IO
Name	Active Level	Description	Relevant Protocols										
CLK	Edge	This differential Input is used to generate the bit-rate clock for the PHY transmitter and receiver. Specs for this clock signal (frequency, jitter, ...) are implementation dependent and must be specified for each implementation. This clock may have a spread spectrum modulation.	PCIe, SATA, USB, DisplayPort, Converged IO										
PCLK	Rising Edge	<p><i>This signal is relevant for "PCLK as PHY Input" mode only.</i></p> <p>All data movement across the parallel interface is synchronized to this clock. This clock operates at a frequency set by PCLK Rate. The rising edge of the clock is the reference for all signals. Spread spectrum modulation on this clock is allowed.</p>	PCIe, SATA, USB, DisplayPort, Converged IO										

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	Name	Direction	Active Level	Description
	CLK	Input	Edge	This Input is used to generate the bit-rate clock for the PHY transmitter and receiver. Specs for this clock signal (frequency, jitter, ...) are implementation dependent and must be specified for each implementation. This clock may have a spread spectrum modulation.
	PCLK	Output	Rising Edge	Parallel interface data clock. All data movement across the parallel interface is synchronized to this clock. This clock operates at 125MHz, 250MHz, or 500 MHz depending on the Rate control input and the data interface width. The rising edge of the clock is the reference for all signals. Spread spectrum modulation on this clock is allowed.
<p><i>PHY Interface for the PCI Express Architecture, Version 2.00 (2007) (available at http://www.applistar.com/wp-content/uploads/apps/pipe2_00.pdf), at 16.</i></p> <p>Additionally, PLLs are often used within the PCIe PHY as part of the clock and data recovery (CDR) functionality of the receiver.</p>				

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	<p style="text-align: center;">Figure 5. Serial System SerDes Block Diagram</p>

A System Designer's Guide for Building a PCIe Clock Tree while Addressing Timing Challenges, Application Note AND9202/D, ON Semiconductor (available at <https://www.onsemi.com/pub/Collateral/AND9202-D.PDF>), at 5.

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	<p>The PLL clock circuitry in the PCIe PHY in each Sony CXD processor also generates different clock frequencies based on PCIe version and the associated data transfer rate. The PLL clock circuitry, e.g., the transmit (TX) PLL, multiplies the reference clock frequency to achieve the desired data rate. This standard approach is consistent with the discussion below.</p> <div style="border: 1px solid black; padding: 10px; margin-top: 10px;"> <p>3. Refclk and Clocking Architectures</p> <p>An external clock reference clock (Refclk) is required for transmitting data between two PCIe devices. A Refclk frequency of 100 MHz ±300 ppm is specified for all three line rates (2.5 Gbps, 5.0 Gbps, 8.0 Gbps). The burden has been placed on the TX PLL to multiply the 100 MHz Refclk frequency to the desired data rate. Although the Refclk frequency has remained the same, the jitter performance requirements of the Refclk have improved to support the higher data rates prevalent with PCI Express 2.1 and 3.1. We will look at the Refclk jitter requirements in the following sections.</p> </div> <p><i>Silicon Labs AN562, PCI Express 3.1 Jitter Requirements (Rev. 0.2 11/15) (available at https://www.silabs.com/documents/public/application-notes/AN562.pdf), at 3.</i></p> <p>The interface controller in each Sony CXD processor, e.g., the CXD90059GB processor in the PlayStation 4 Slim, thus conveys the PCI bus transaction through the LVDS channel based on different clock frequencies.</p>
2. The computer of claim 1 wherein the interface controller conveys the PCI bus transaction through the LVDS channel based on a selected frequency of the different clock frequencies.	<p><i>See claim 1, above.</i></p> <p>The interface controller in each Sony CXD processor in the PlayStation 4, e.g., the CXD90059GB processor in the PlayStation 4 Slim, conveys the PCI bus transaction through the LVDS channel based on a selected frequency of the different clock frequencies.</p> <p>The PLL within the PCIe PHY will select one bit rate frequency based on the version of the PCIe protocol and the highest common data rate used for the link.</p>